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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,354	03/09/2000	Roy Glenn Musselman		3096

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EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	6

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/522,354	Applicant(s) MUSSELMAN ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- Th MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3-09-2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-14 have been presented for examination. Claims 1-14 have been examined and rejected.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Applicant is directed to see figure 8 of reference *Beausoleil et al. U.S. Patent 5,551,013.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Beausoleil et al. U.S. Patent 5,551,013** in view of **DeHon et al. U.S. Patent 5,742,180.**

3.1 As regards **Claims 1 and 9** the *Beausoleil et al.* reference discloses; a chip module for an emulation system **(Figures 1-8),** a plurality of logic cells **(Figures 10, 11),** a plurality of input lines **(Figure 7),** a configurable logic function memory element **(Figure 3B),**

specifying a logic function of said plurality of input lines **(Figures 1, 2A, 2B, 3A),** that produces an output **(Figures 7 and 10).**

The *Beausoleil et al.* reference does not expressly disclose configurable interconnect logic said configurable interconnection logic routing the output of any cell to an input of any other cell, the plurality of cells arraigned in rows and columns and sequential signals corresponding to a row of cells and controlling propagation of logic signals through the cells of that row.

The *DeHon et al.* reference discloses configurable interconnect logic said configurable interconnection logic routing the output of any cell to an input of any other cell, the plurality of cells arraigned in rows and columns and sequential signals corresponding to a row of cells and controlling propagation of logic signals through the cells of that row **(Figure 2B, 2C, 2D, 3A, 3B, 4A, 5A, 5B, 5C, 6A, 6B, 6C, Col. 2 Lines 10-67, Col. 3 Lines 13-30, Col. 4 Lines 31-60).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Beausoleil et al.* reference with the *DeHon et al.* reference because *(motivation to combine)* the *Beausoleil et al.* reference discloses a method to provide flexible interconnect between multiple logic cells ***(DeHon et al. Col. 4 Lines 46-52).***

3.2 As regards **Claims 2 and 10** the *Beausoleil et al.* reference does not expressly disclose a multiplexer.

The *DeHon et al.* reference discloses a multiplexer **(Col. 4 Lines 11-15).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Beausoleil et al.* reference with the *DeHon et al.* reference

because *(motivation to combine)* the *Beausoleil et al.* reference discloses a method to provide flexible interconnect between multiple logic cells ***(DeHon et al. Col. 4 Lines 46-52).***

3.3 As regards **Claims 3, 4, 11 and 12** the *Beausoleil et al.* reference does not expressly disclose delay logic.

The *DeHon et al.* reference discloses delay logic **(Figure 2B, Col. 7 Lines 55-67, Col. 8 Lines 1-3).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Beausoleil et al.* reference with the *DeHon et al.* reference because *(motivation to combine)* the *Beausoleil et al.* reference discloses a method to provide flexible interconnect between multiple logic cells ***(DeHon et al. Col. 4 Lines 46-52).***

3.4 As regards **Claims 5-8, 13 and 14** the *Beausoleil et al.* reference discloses inputs **(Figure 11A)** and outputs **(Figure 10).**

The *Beausoleil et al.* reference does not expressly disclose a strobe (control signal for latching up a signal) or time multiplexing or memory elements feeding into the cell array.

The *DeHon et al.* reference discloses strobe signals **(Figure 5C, Col. 5 Lines 61-64),** and time multiplexing **(Col. 4 Lines 11-15)** and memory elements feeding into the cell array **(Figure 4B).**

Conclusion

4.

4.1 The Examiner takes note that the *Trimberger* reference entitled, *"Scheduling Designs into a Time-Multiplexed FPGA"* further illustrates many of the concepts put forward in the *DeHon et al.* reference.

4.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
April 19, 2003

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100